

FIG. 1(a)

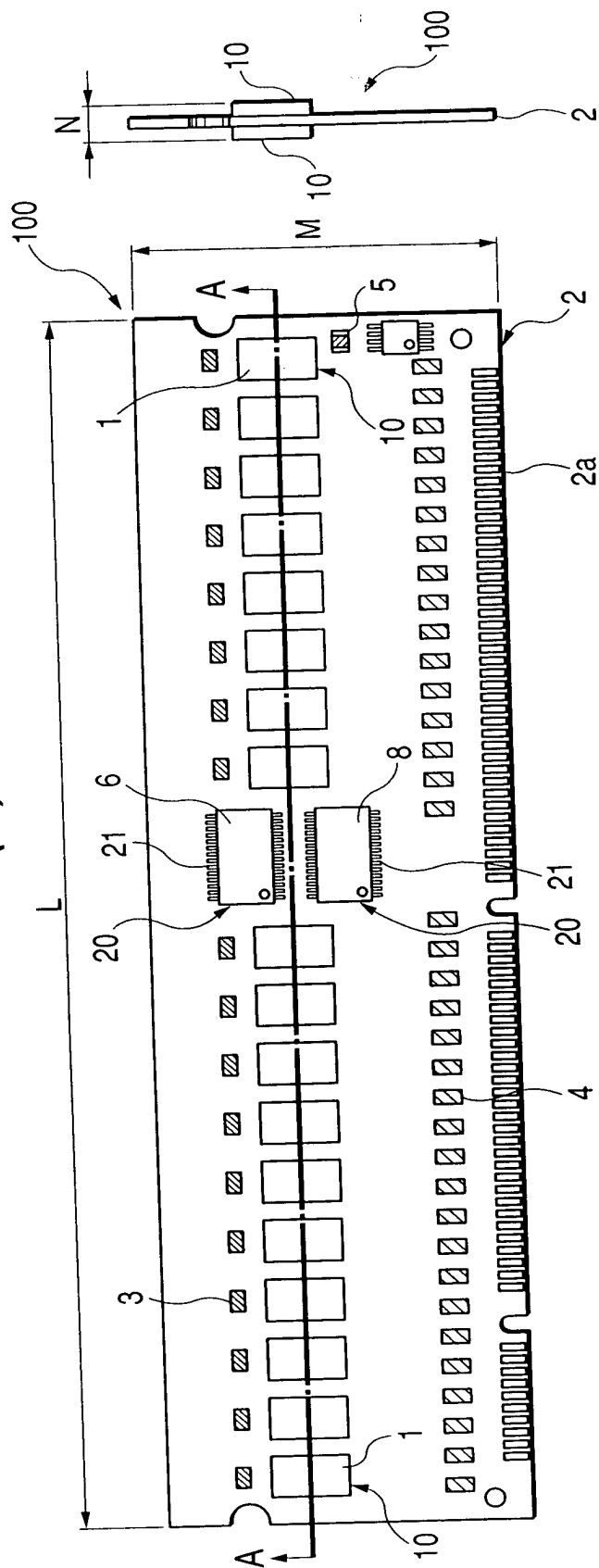


FIG. 1(b)

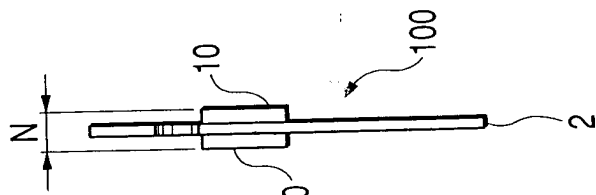


FIG. 1(c)

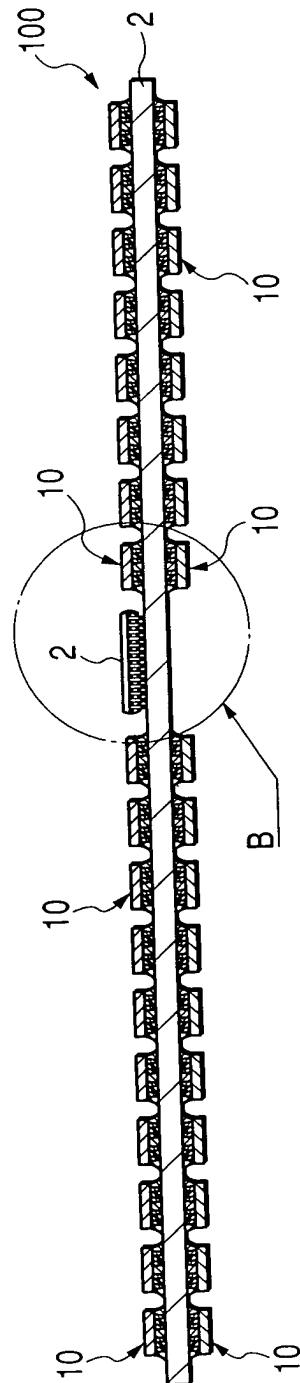


FIG. 3

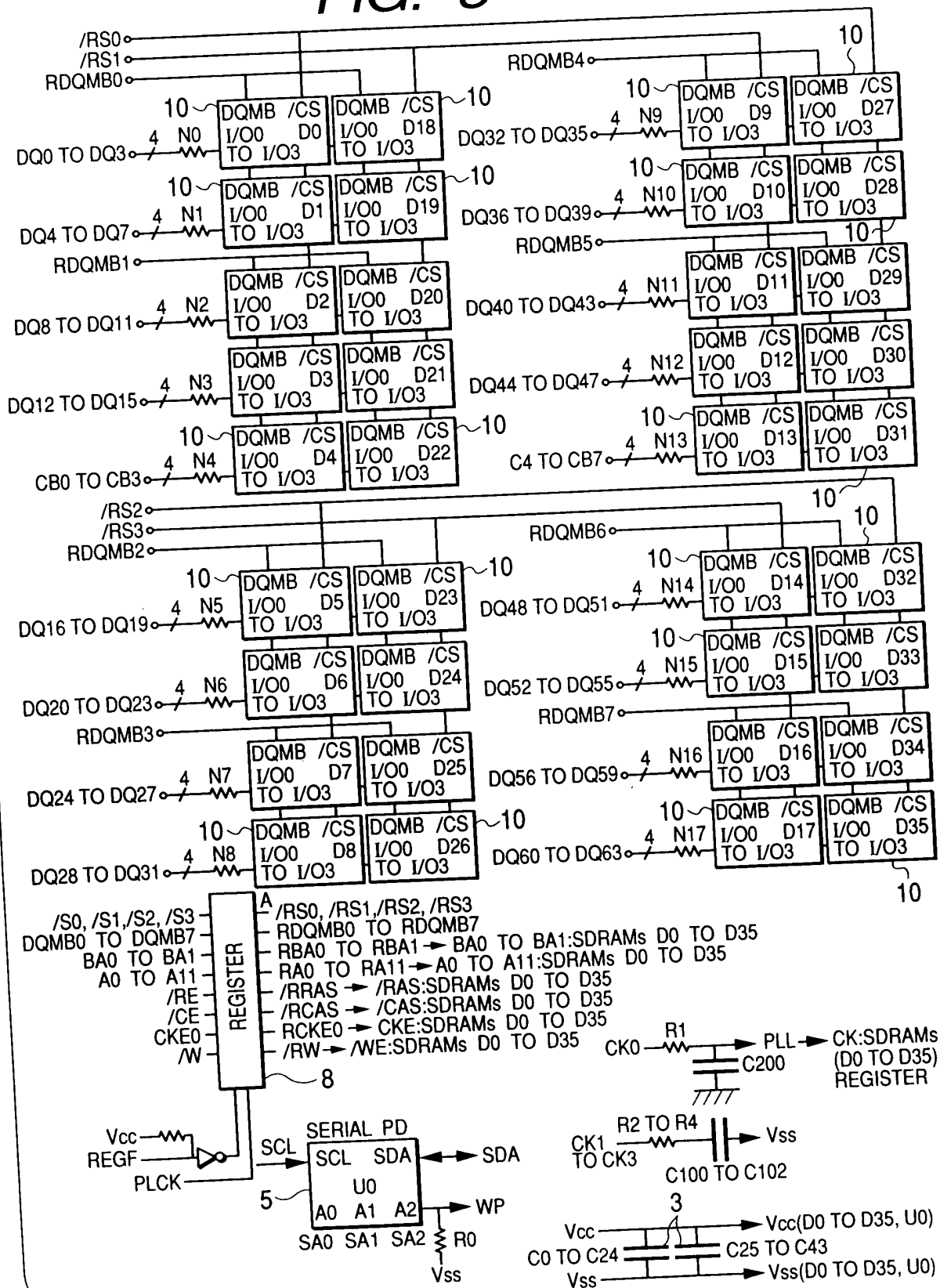


FIG. 4

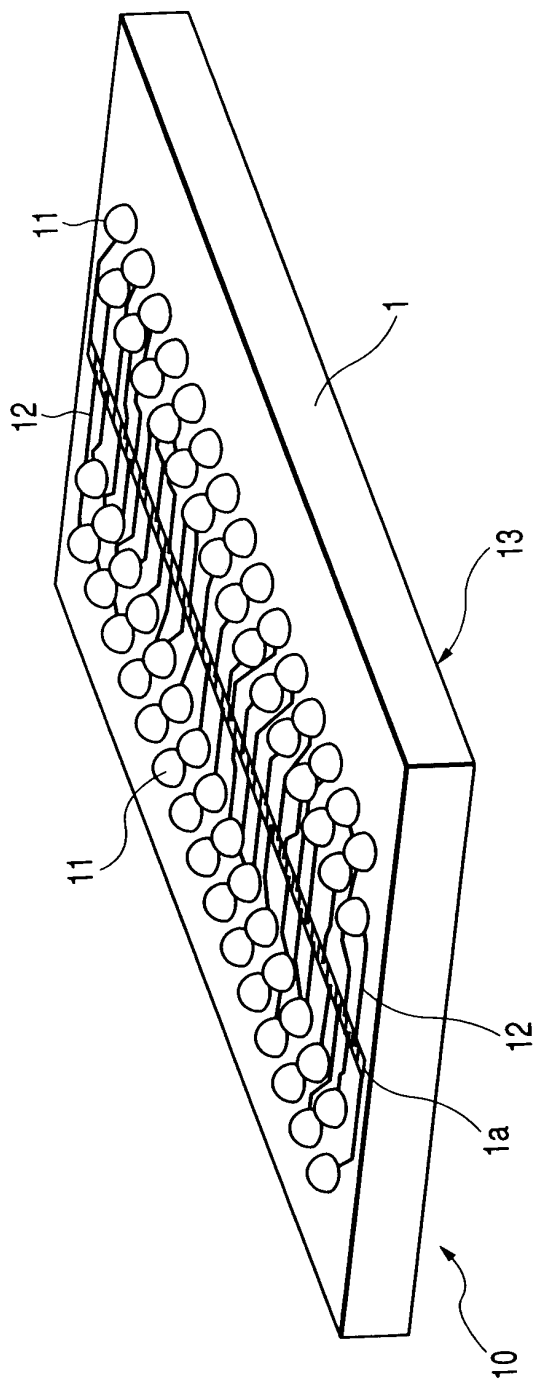
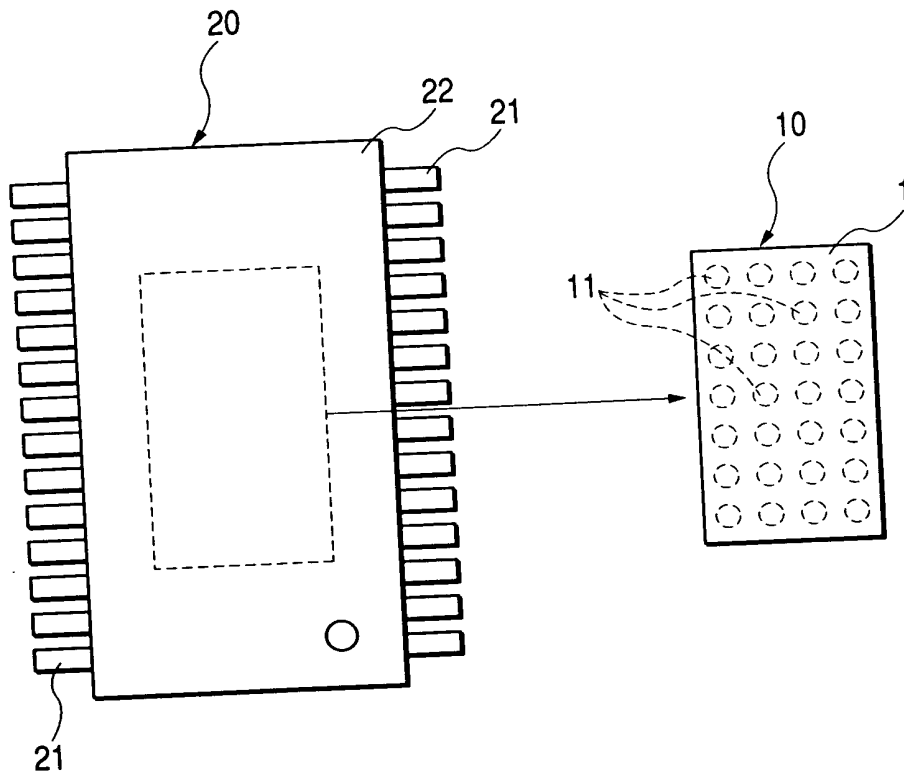


FIG. 5(a)

FIG. 5(b)



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graph TD
    S1[WAFER PROCESS] --> S2[WPP - FORMING FIRST INSULATING LAYER]
    S2 --> S3[WPP - FORMING RE - WIRING LAYER]
    S3 --> S4[WPP - FORMING SECOND INSULATING LAYER]
    S4 --> S5[WPP - FORMING UBM]
    S5 --> S6[TEST OF WAFERS (W - TEST)]
    S6 --> S7[TEST BY PROBE (P - TEST 1)]
    S7 --> S8[LASER BLOWN FUSES]
    S8 --> S9[TEST BY PROBE (P - TEST 2)]
    S9 --> S10[MARKING ON BACK SURFACE OF THE WAFER]
    S10 --> S11[FORMING OF BUMPS]
    S11 --> S12[DICING]
    S12 --> S13[AGING (BI)]
    S13 --> S14[CHIP SORTING]
  
```

FIG. 7(a)

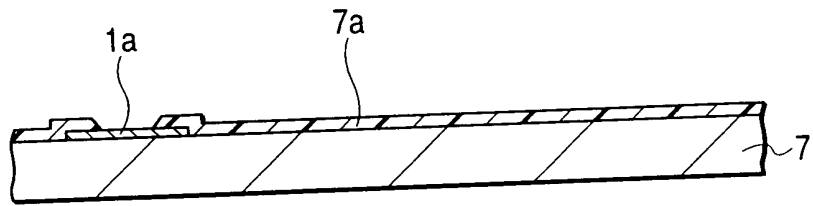


FIG. 7(b)

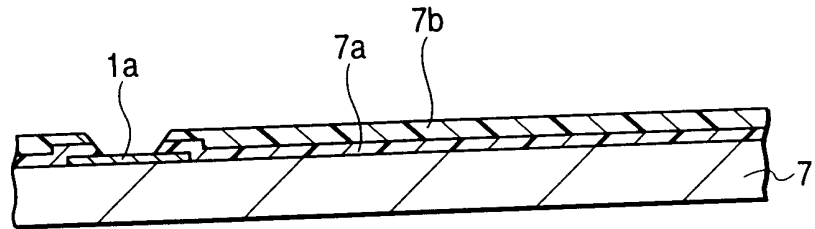


FIG. 7(c)

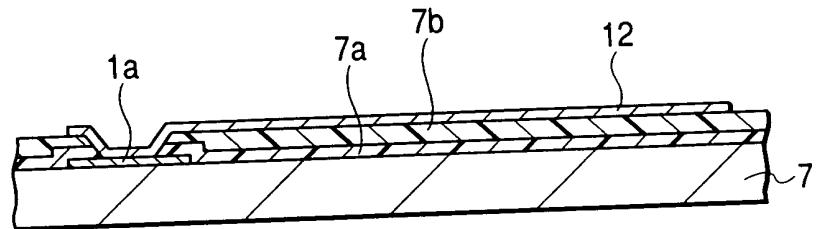


FIG. 7(d)

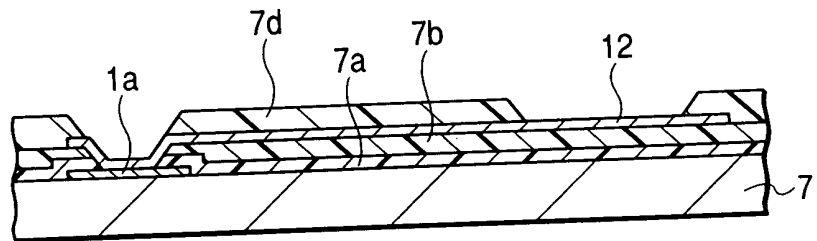


FIG. 7(e)

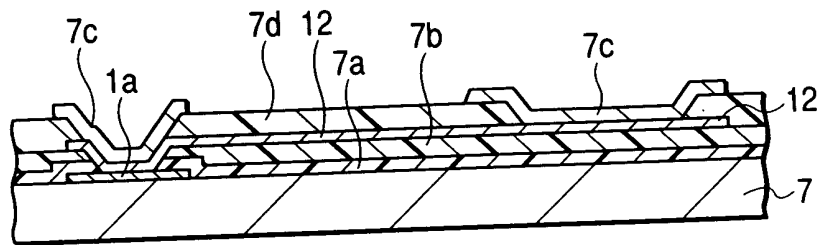


FIG. 7(f)

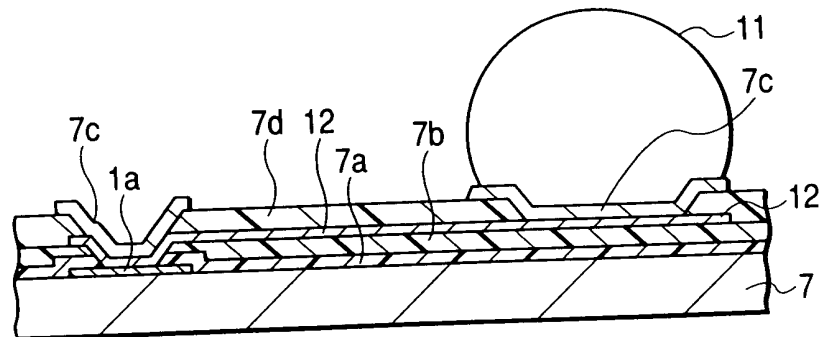


FIG. 8

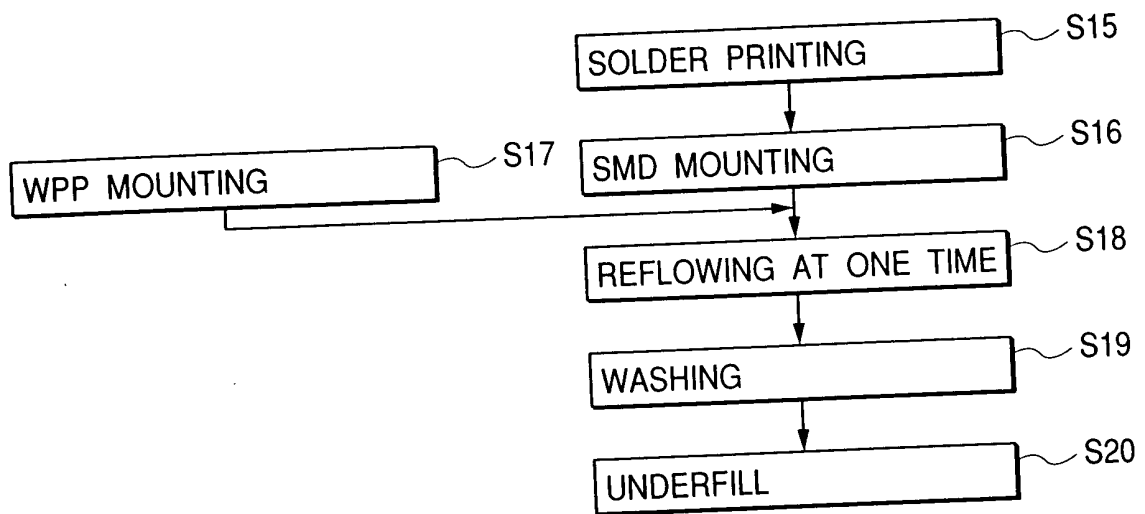
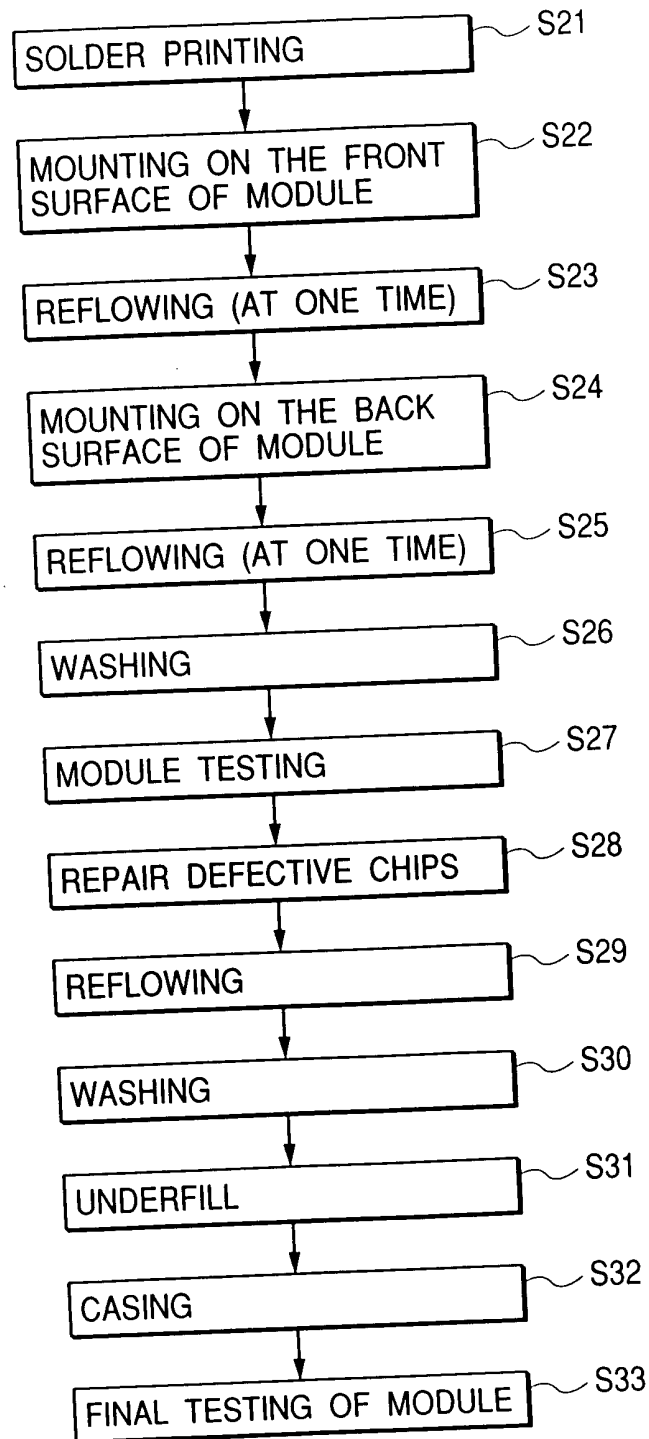


FIG. 9

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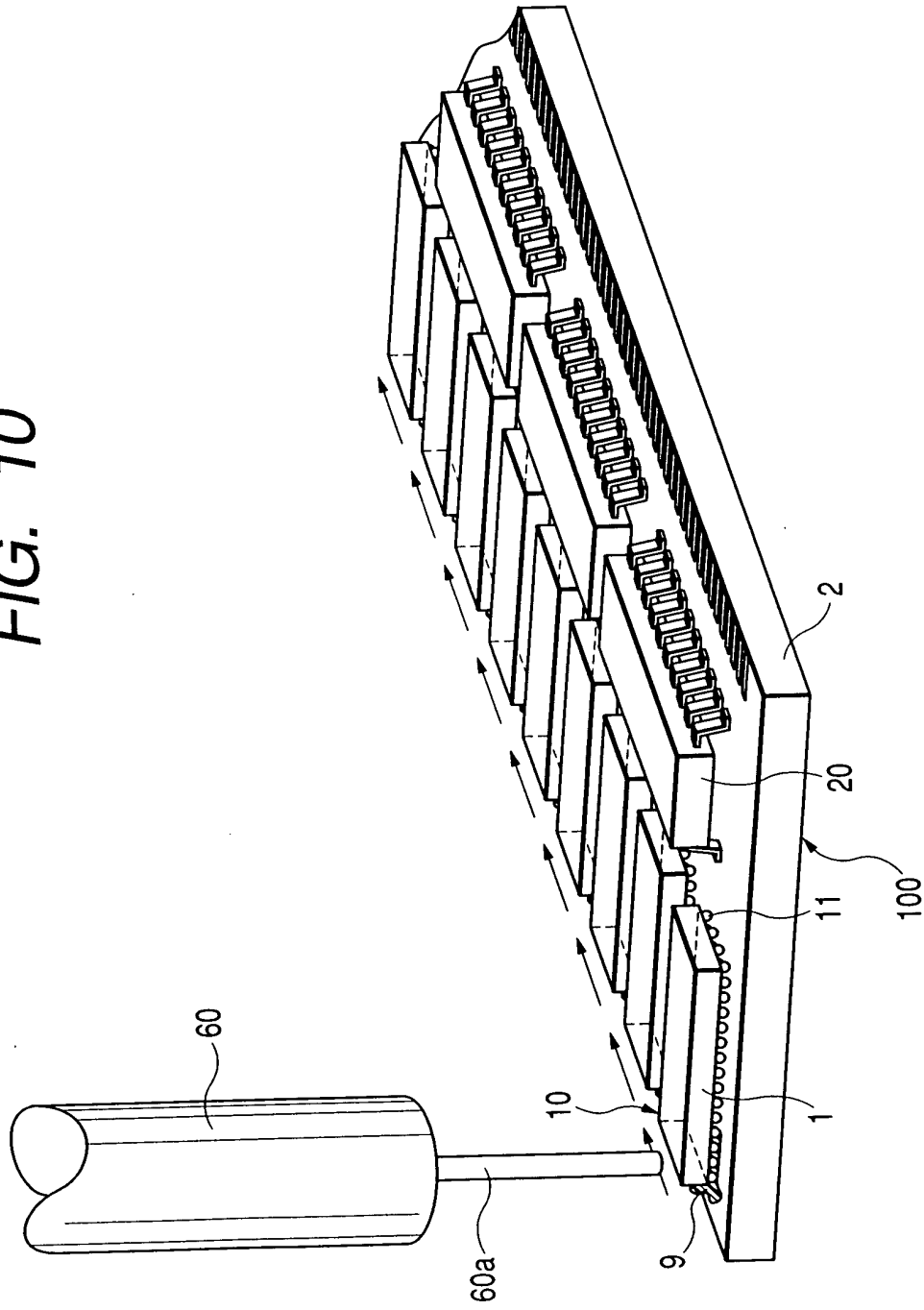


FIG. 10

FIG. 11(a) FIG. 11(c) FIG. 11(e) FIG. 11(g)

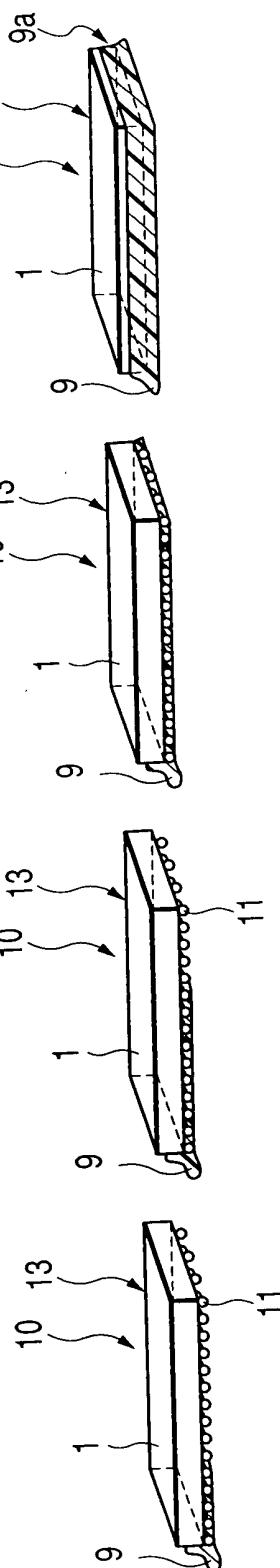
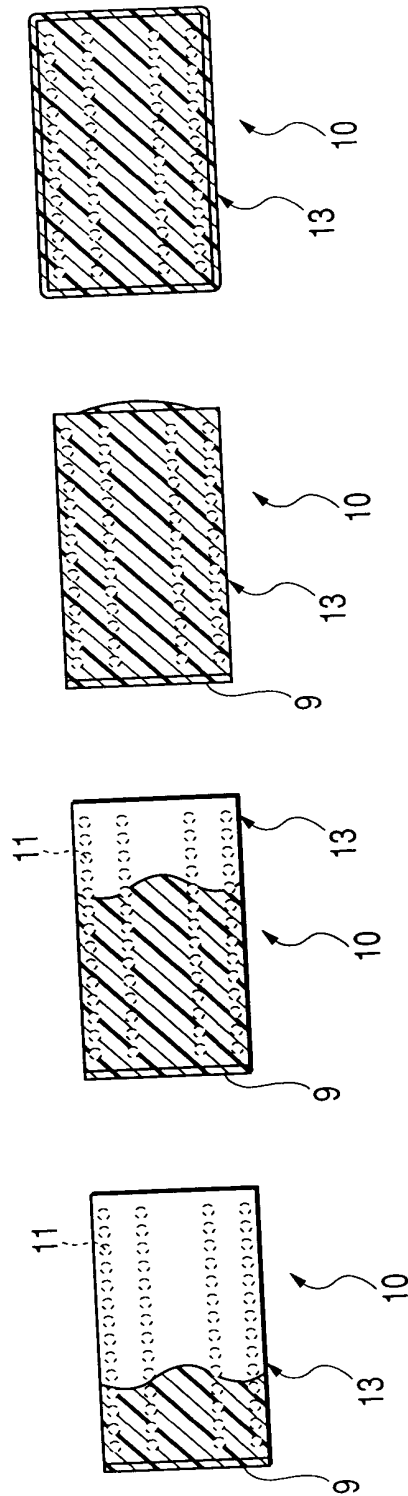


FIG. 11(b) FIG. 11(d) FIG. 11(f) FIG. 11(h)



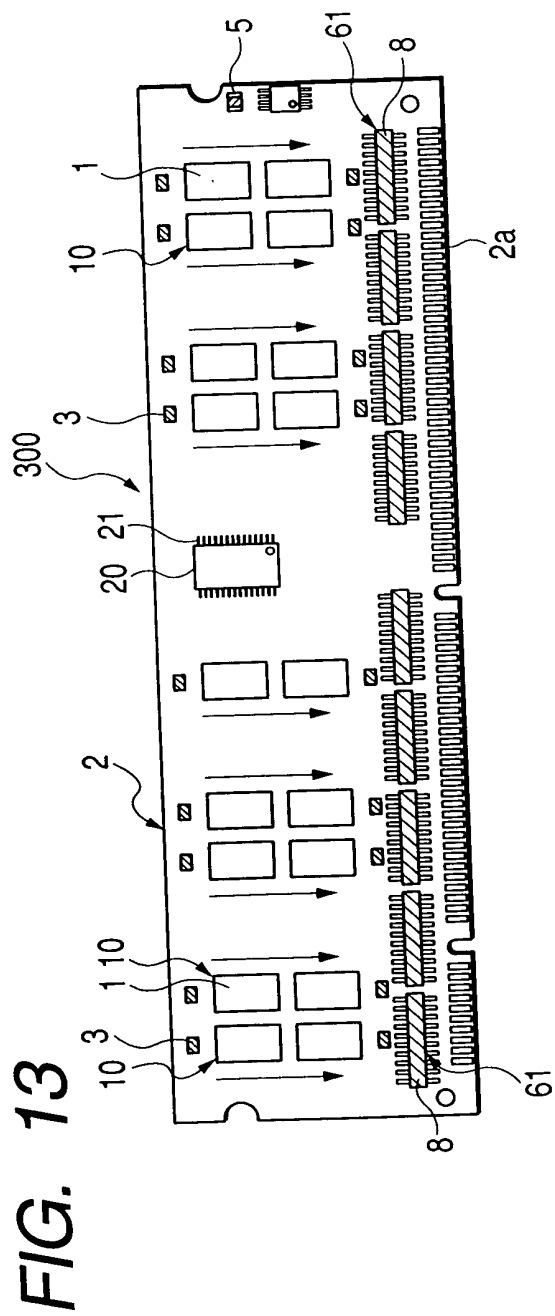
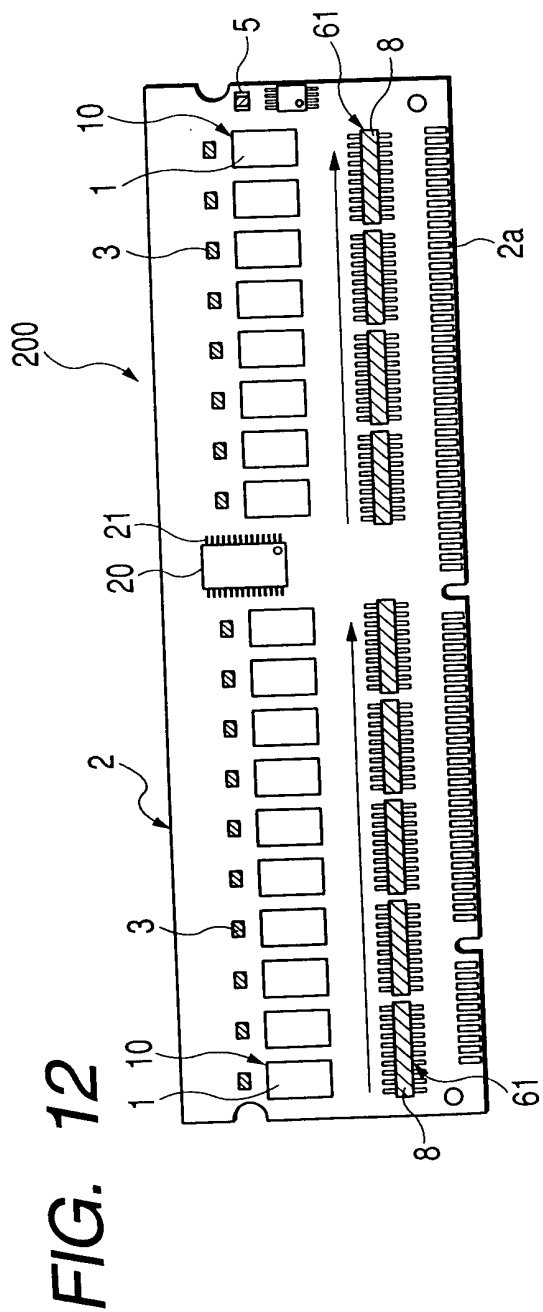


FIG. 14(a)

FIG. 14(c)

FIG. 14(e)

FIG. 14(g)

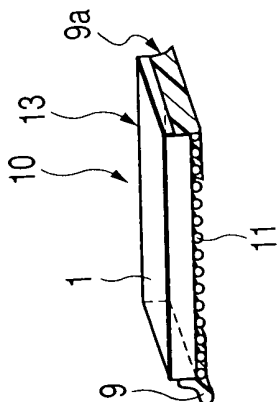
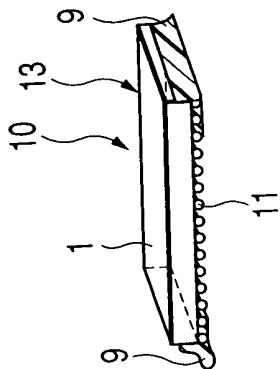
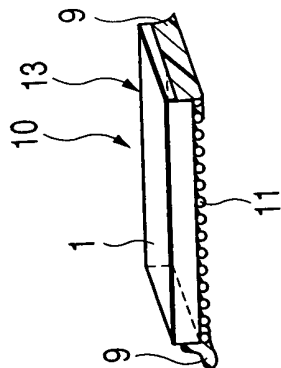
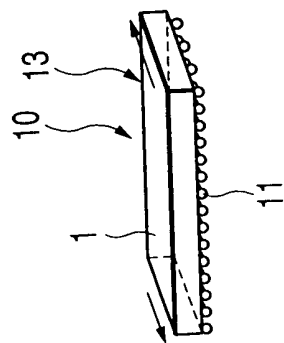


FIG. 14(b)

FIG. 14(d)

FIG. 14(f)

FIG. 14(h)

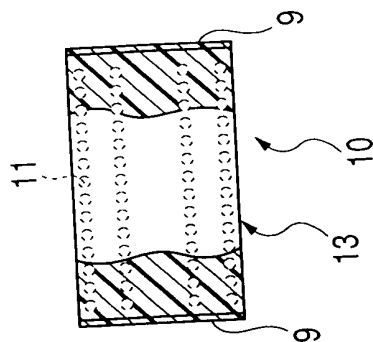
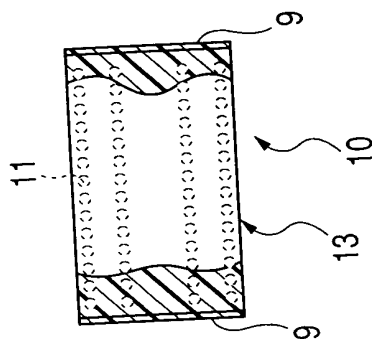
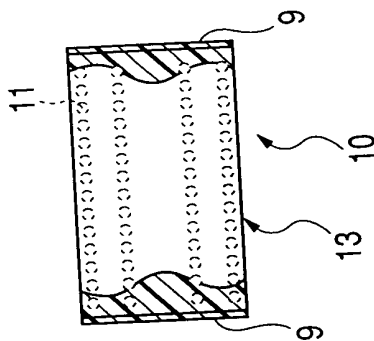
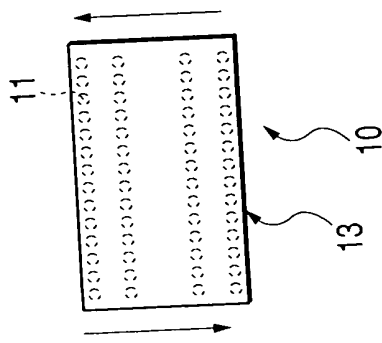


FIG. 15(a)

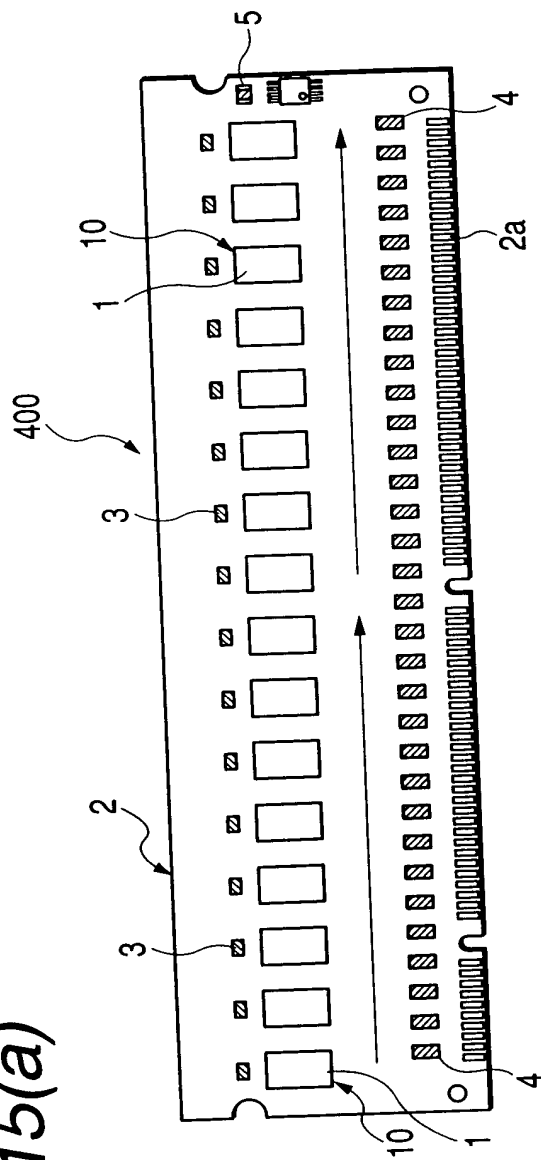
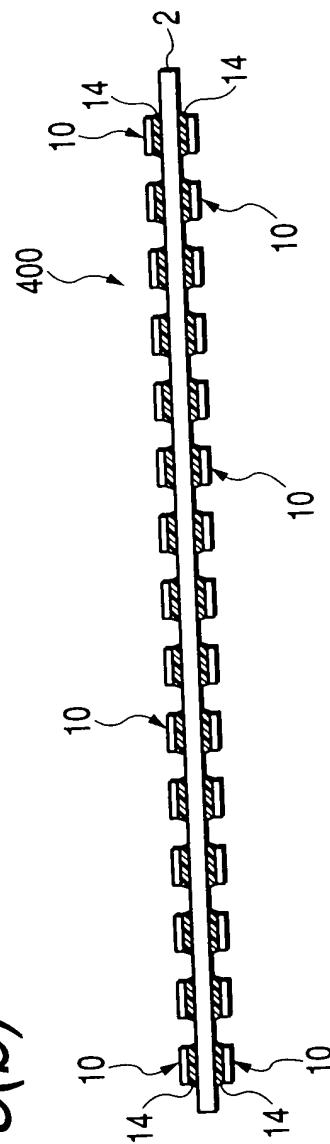


FIG. 15(b)



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FIG. 18

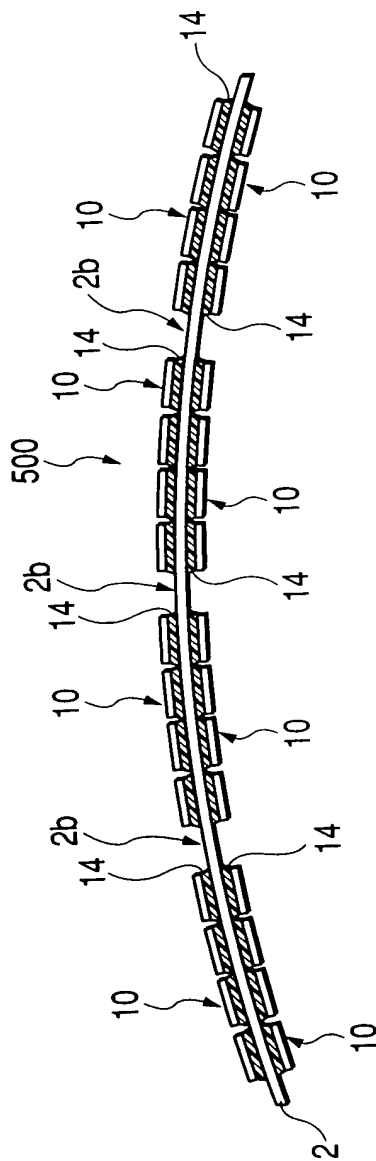


FIG. 19

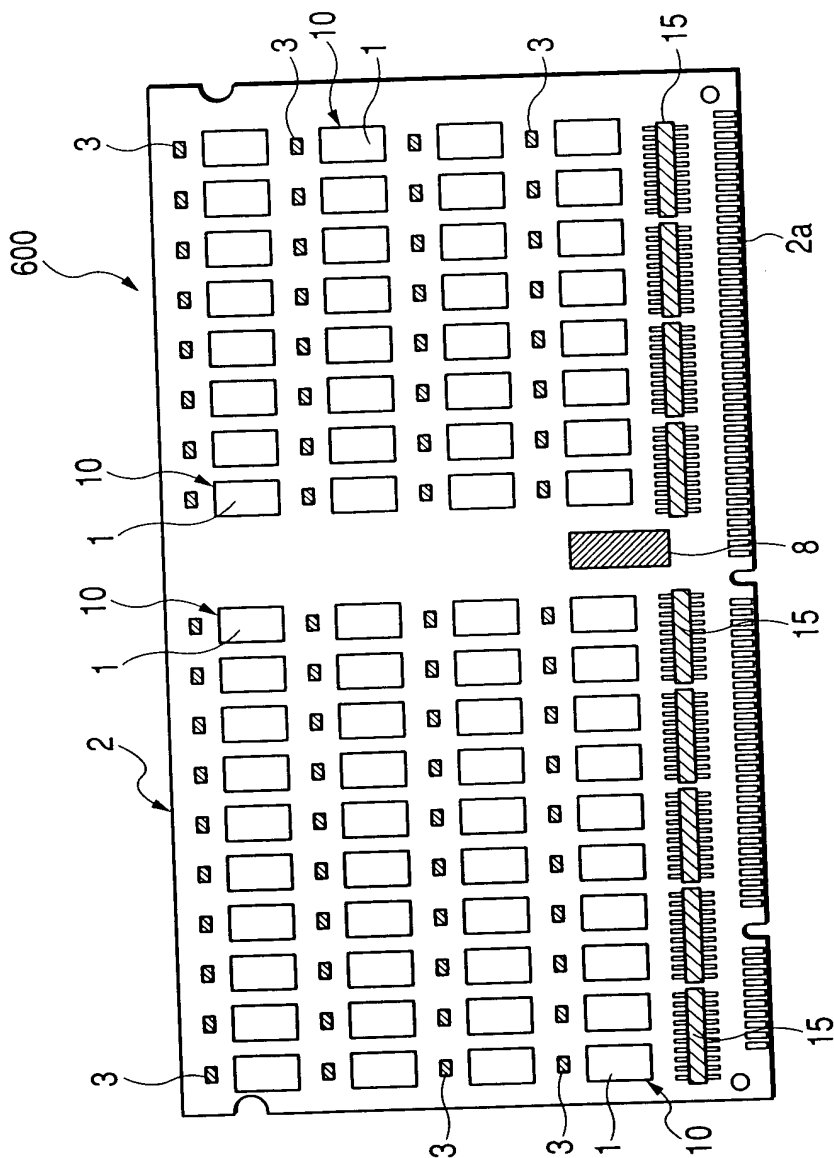


FIG. 20(a)

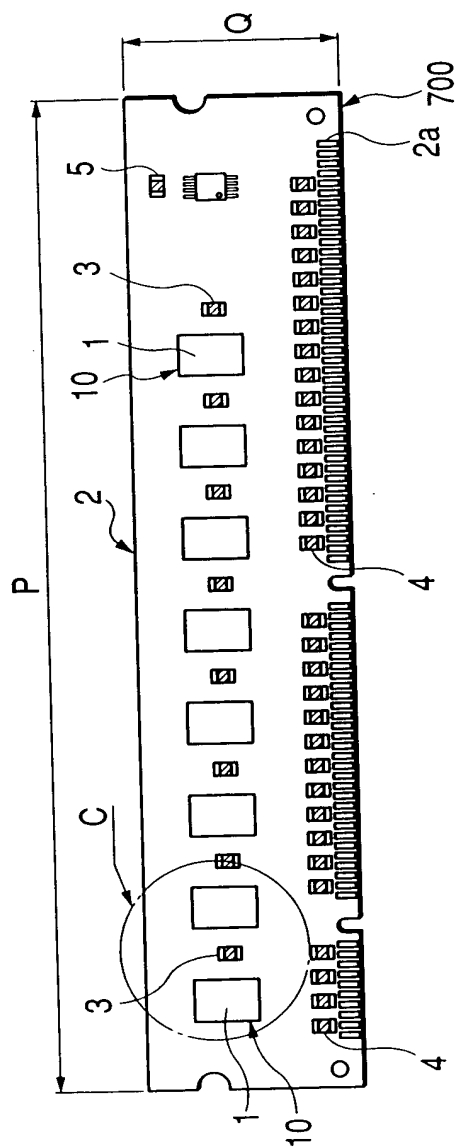


FIG. 20(b)

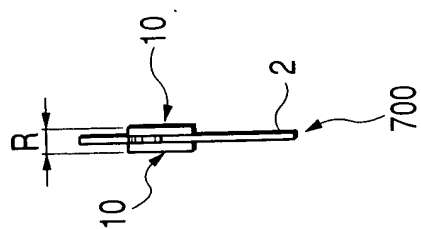


FIG. 22

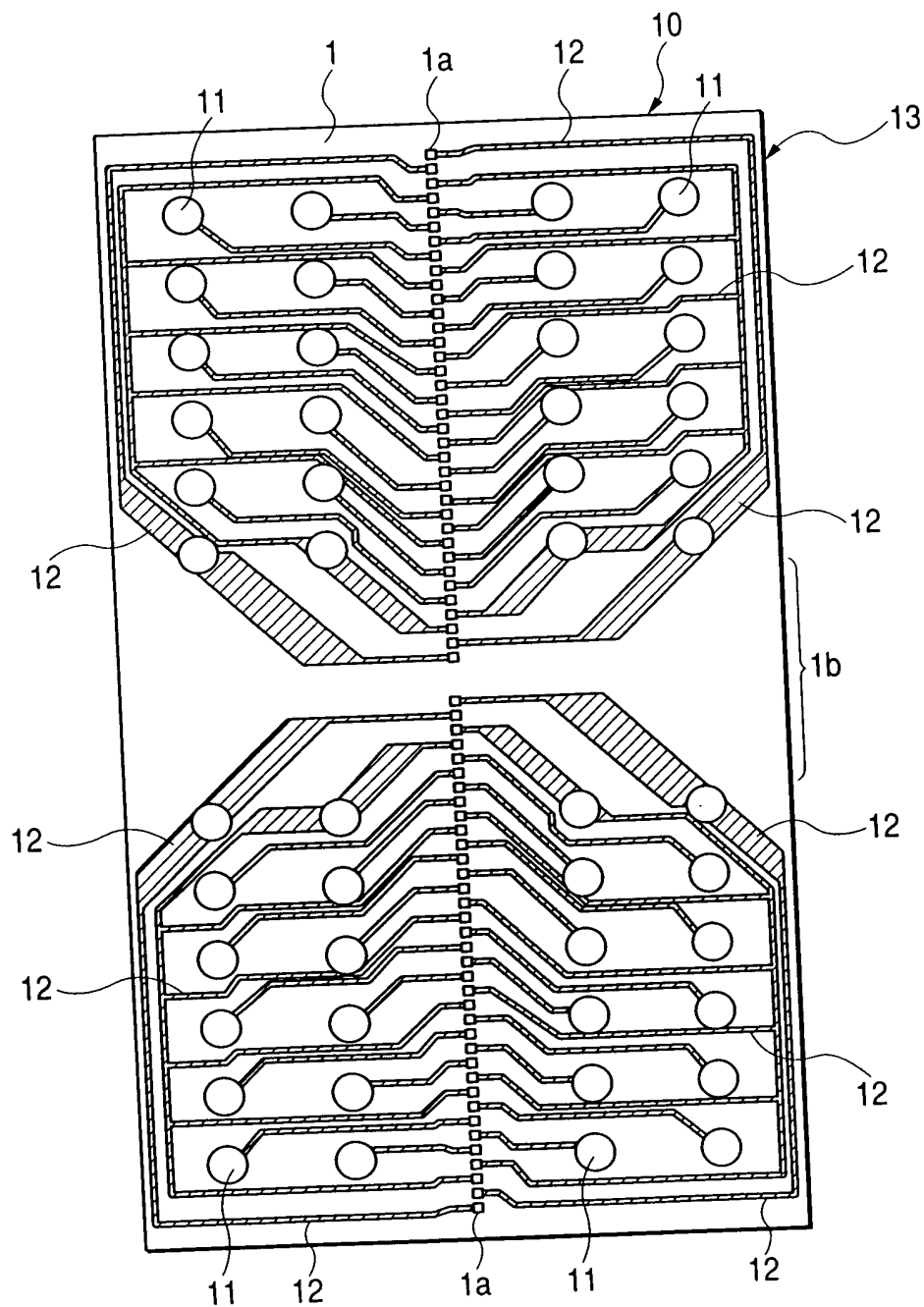
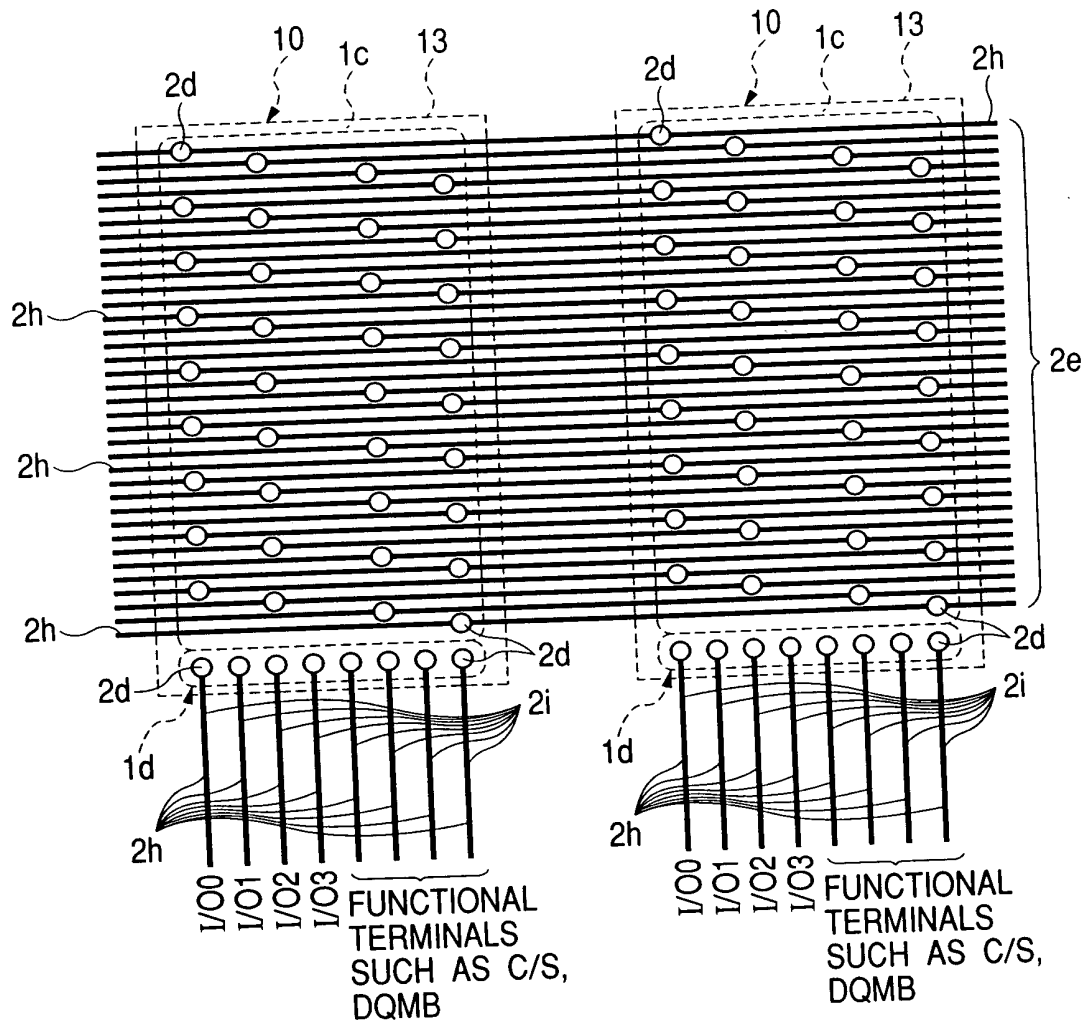
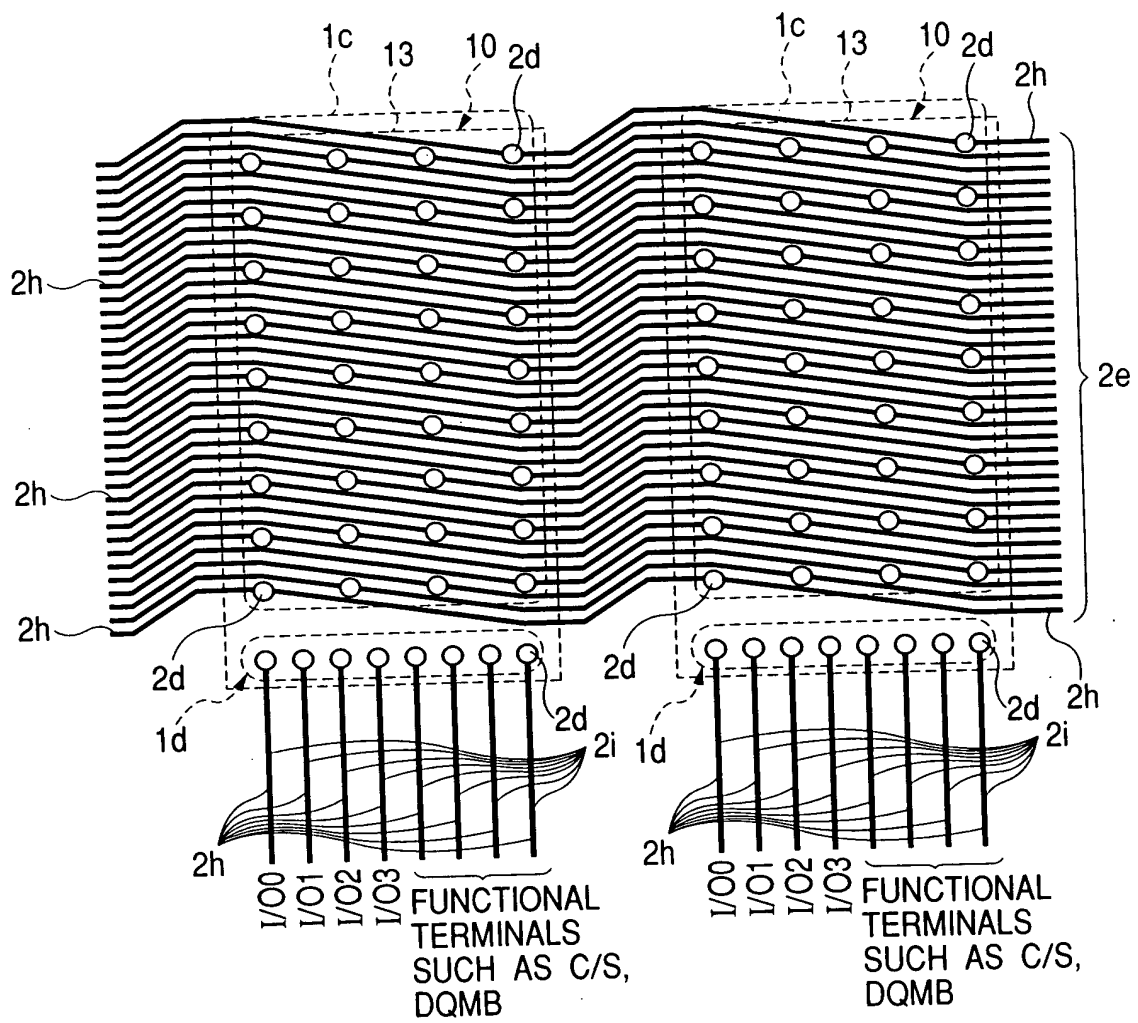


FIG. 24

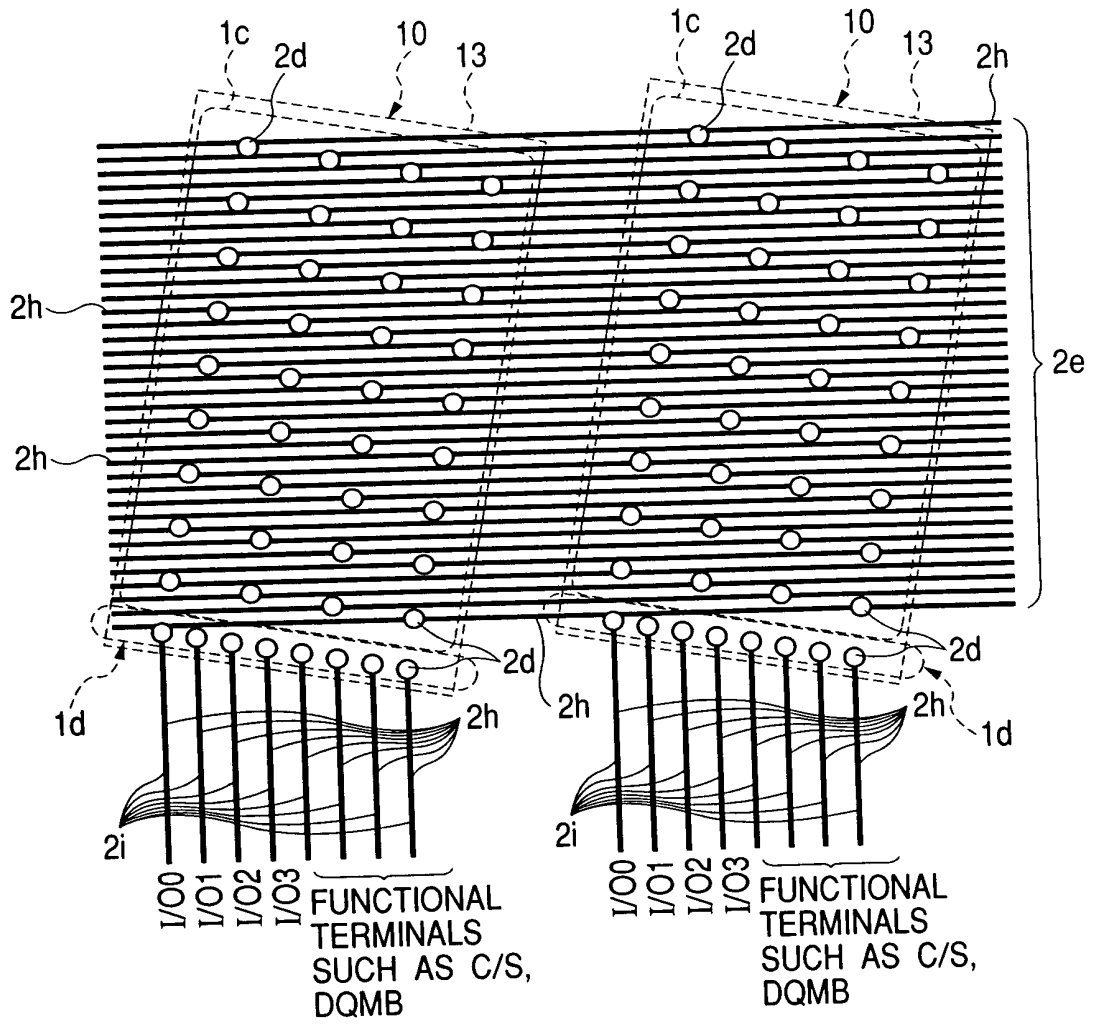


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FIG. 25



00000000000000000000000000000000



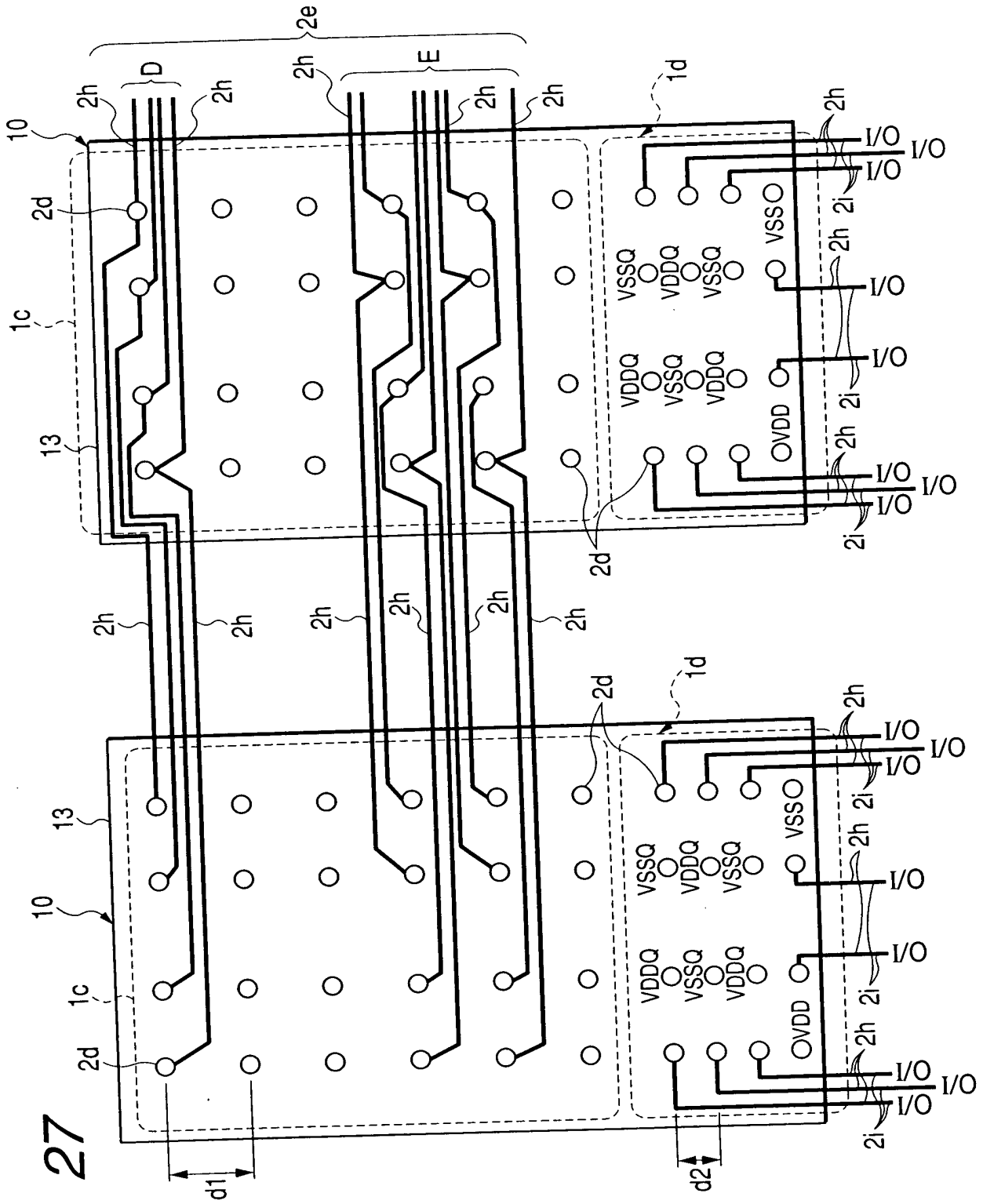


FIG. 27

FIG. 28(a)

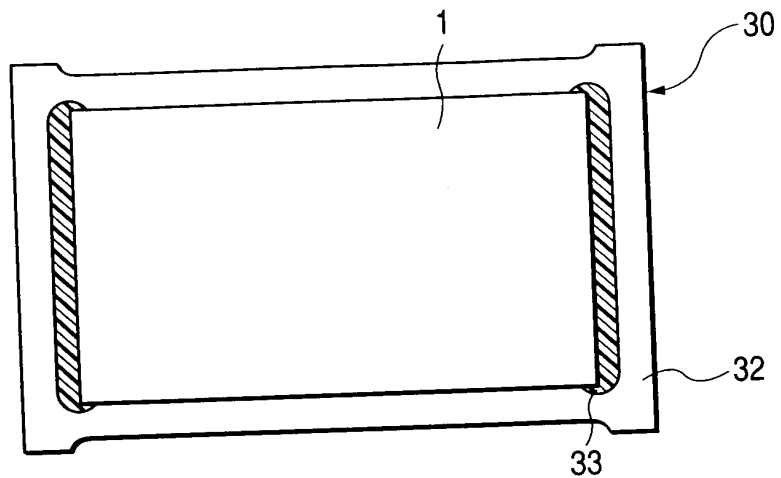


FIG. 28(b)

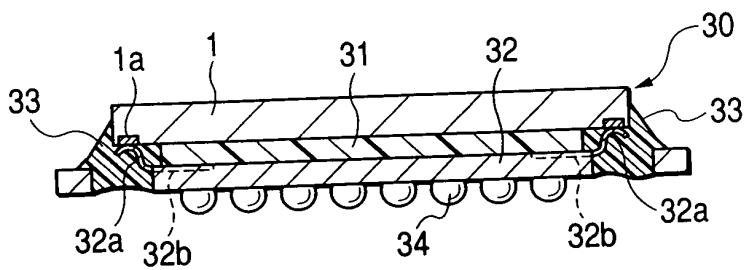
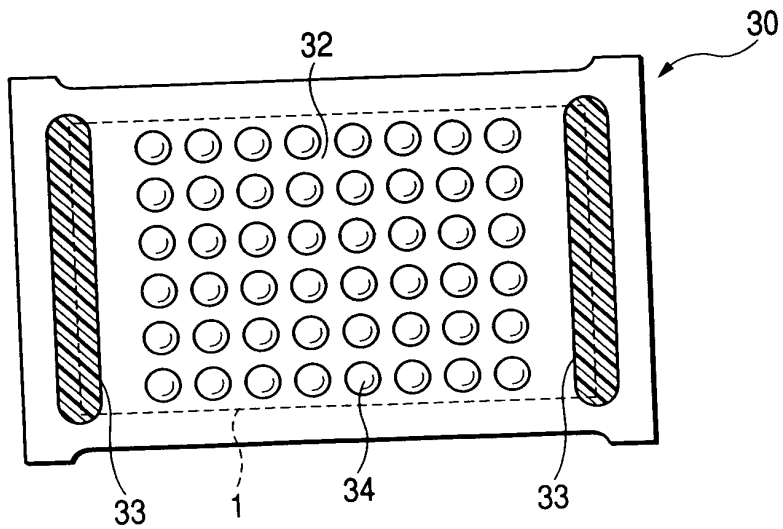


FIG. 28(c)



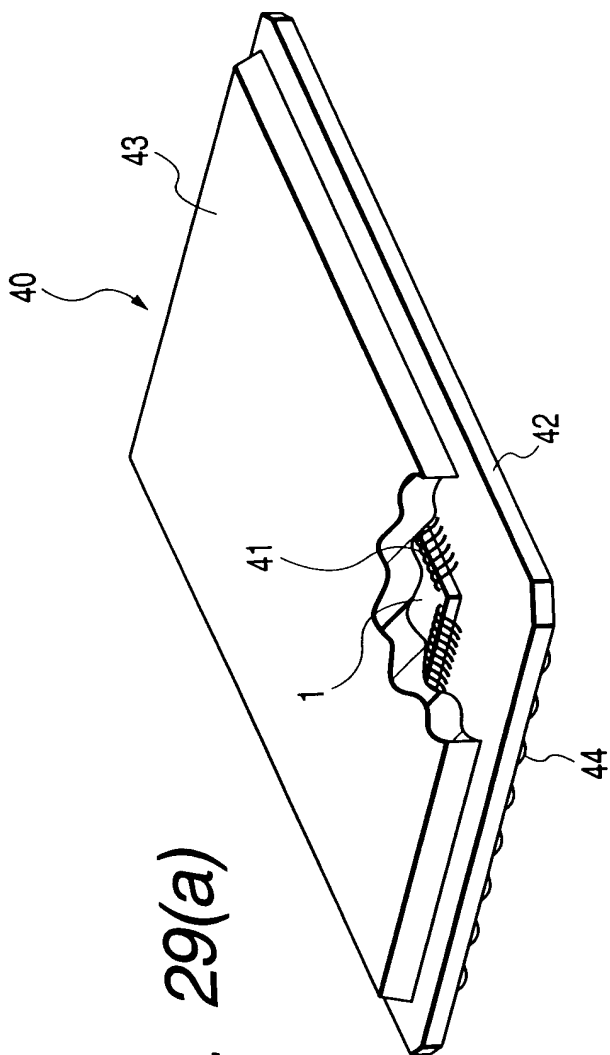


FIG. 29(a)

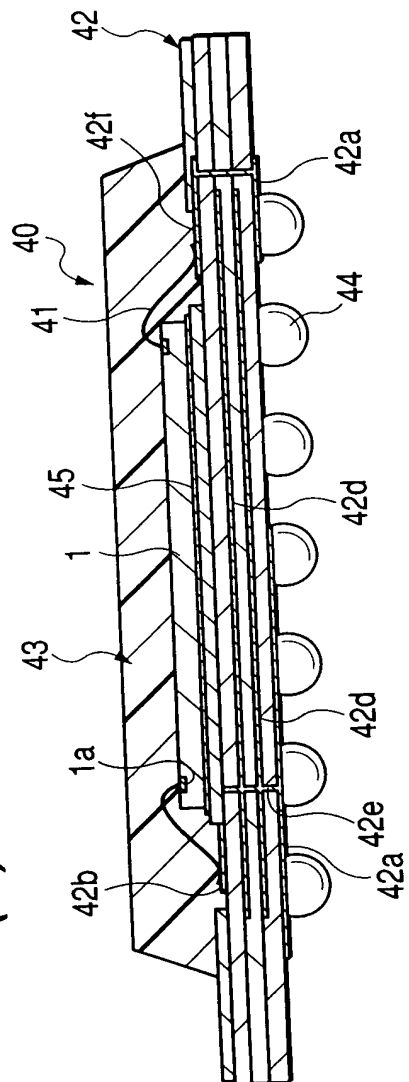


FIG. 29(b)

FIG. 30(a)

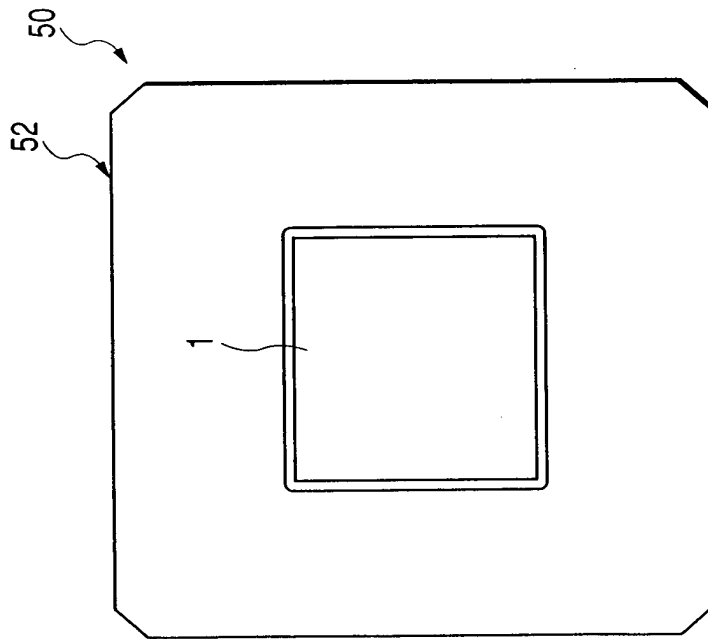


FIG. 30(b)

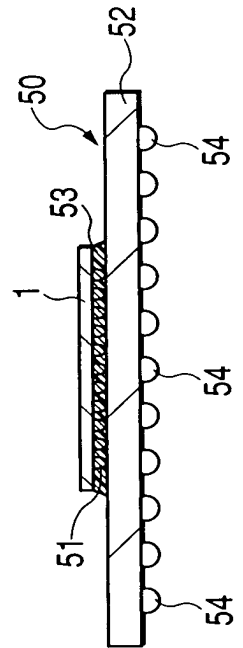


FIG. 30(c)

